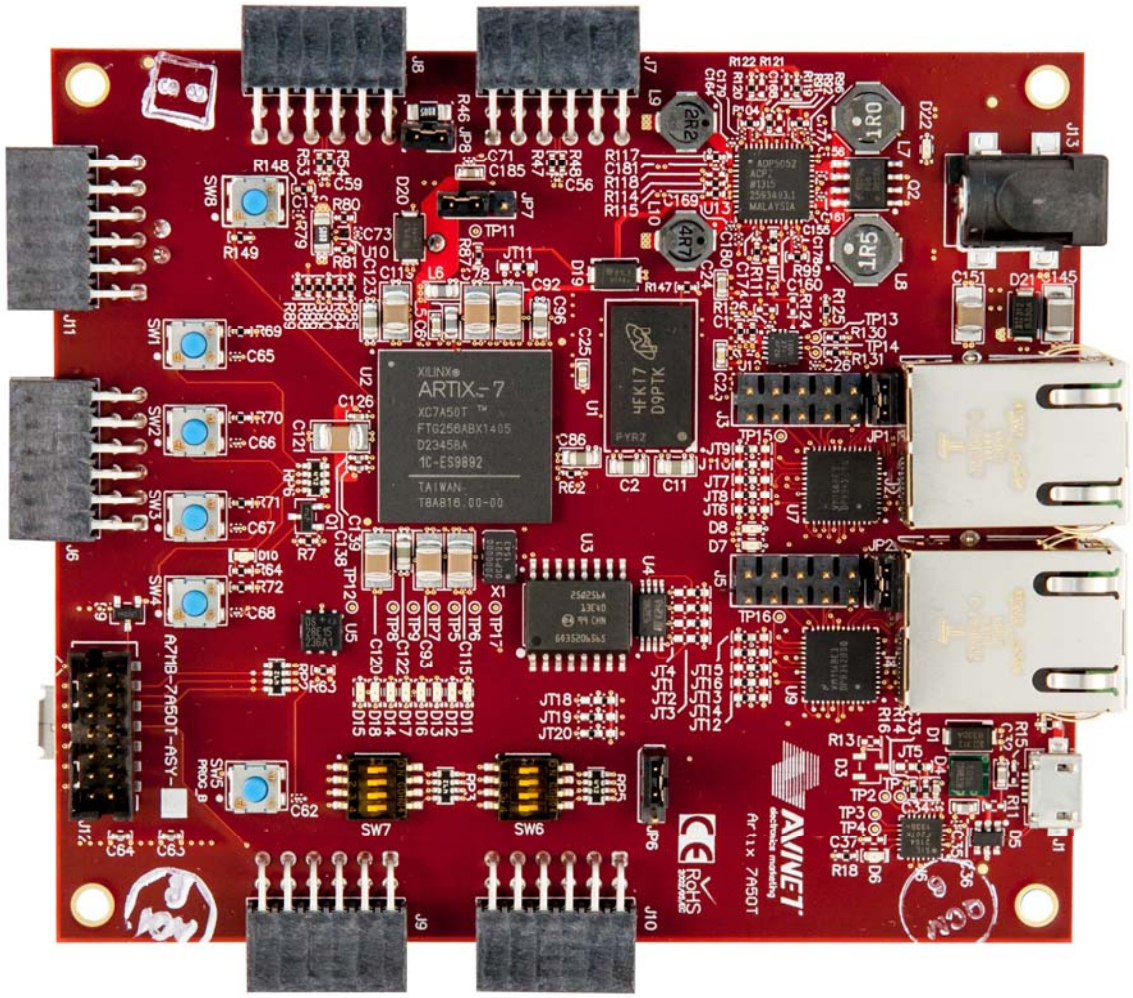
Artix 7A50T

Hardware User Guide



Revision 1.2
11 Dec 2014

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1 Introduction

The Avnet Artix-7A50T board is a low cost, feature rich evaluation platform based on the Xilinx XC7A50T FPGA device in the FTG256 package. The features provided by this board consist of:

- Xilinx XC7A50T-1FTG256C FPGA
- 200 MHz LVCMOS oscillator (system clock)
- 256MB DDR3 SDRAM
- 32MB of QSPI Flash
- 32KB of I2C EEPROM
- Dual 10/100 Ethernet PHY (RMII)
- USB JTAG Programming/Configuration Port
- USB-UART port
- Eight user LEDs (red)
- Two Ethernet status LEDs (red, green)
- Power LED (green)
- FPGA DONE LED (blue)
- Four position DIP switch (user GPIO)
- Four position DIP switch (device address)
- Four user push button switches
- One reset push button switch
- Six PMOD headers
- 512b EEPROM with SHA-256 engine

The Xilinx XC7A50T-1FTG256C device includes the following features:

Device	**XC7A50T-1FTG256C**
Logic cells	52,160
Slices	8,150
CLB Flip Flops	65,200
Maximum Distributed RAM (Kb)	600
Block RAM/FIFO (36Kb each)	75
Block RAM (Kb)	2,700
Clock Management Tiles (CMT)	5
Max Single-ended I/O	250 (170)
Max Differential I/O pairs (not all available in FTG256 package)	120
DSP Slices	120
PCIe Gen 2	1 (0)
AMS/XADC	1
Configuration AES/HMAC blocks	1
Gigabit transceivers	4 (0)

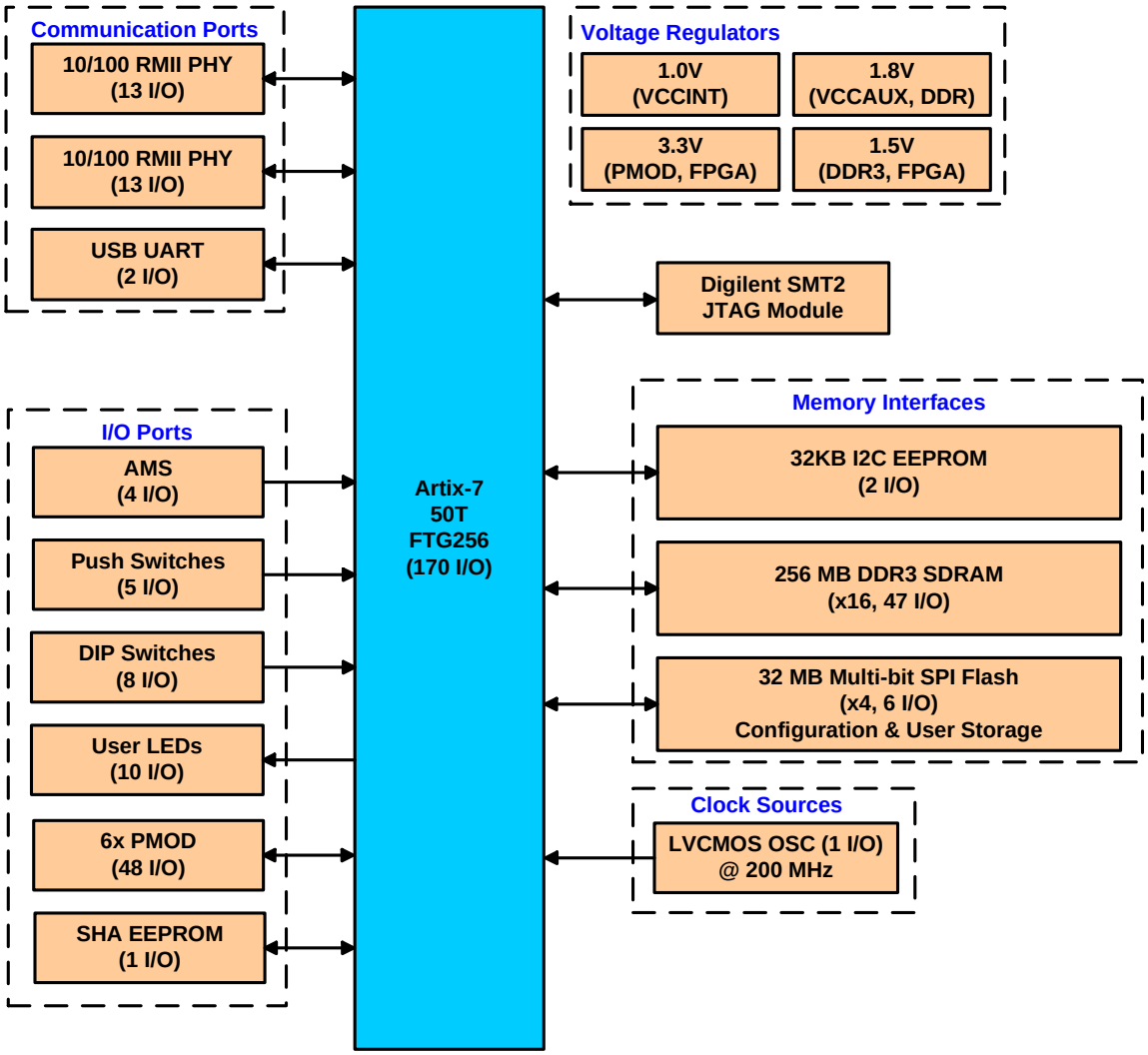

Figure 1 – Artix 7A50T Block Diagram

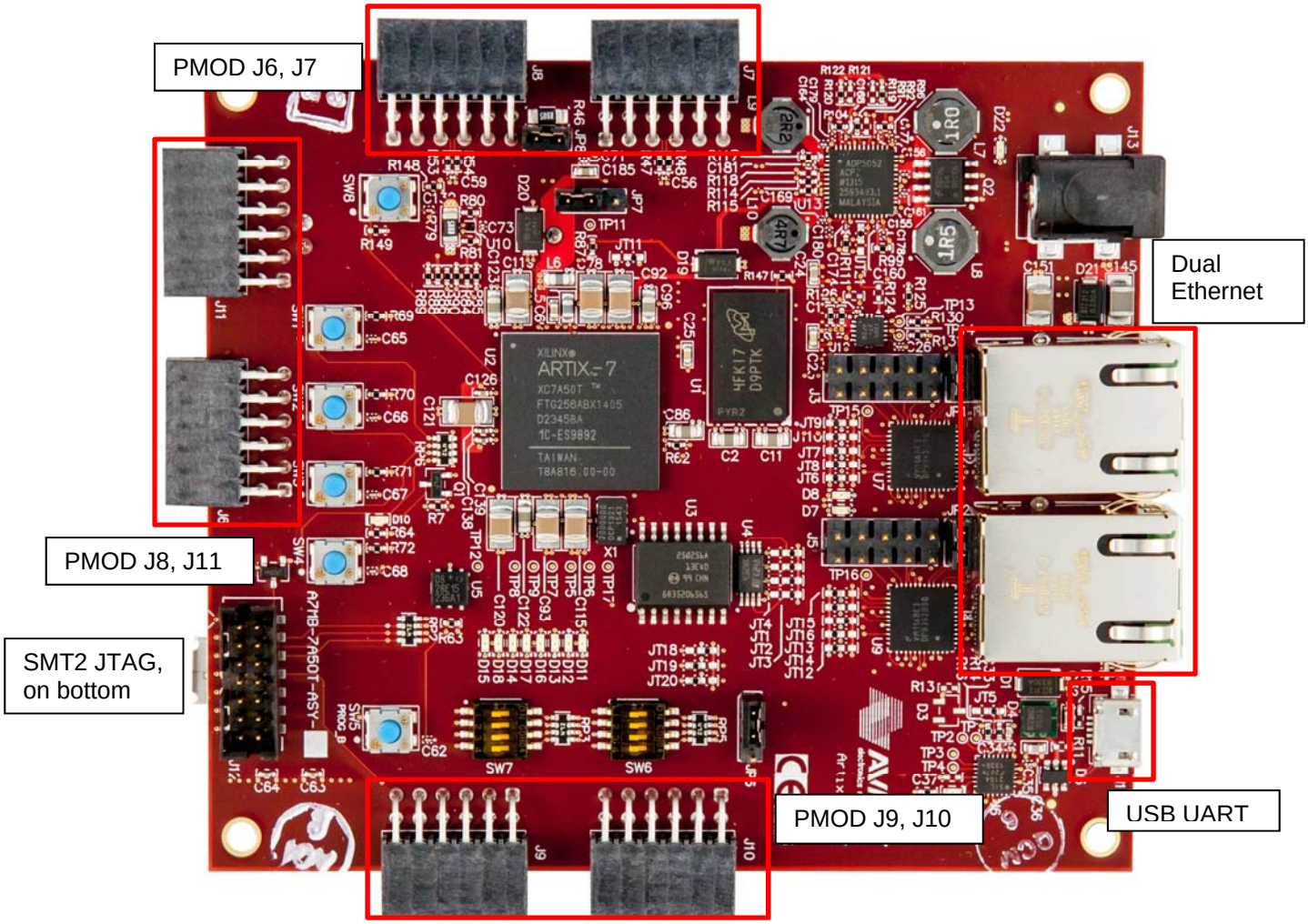

Figure 2: Artix 7A50T Board Functions

2 Functional Description

The following sections provide brief description of each feature provided on the Avnet Artix 7A50T board. For more detailed information regarding specific IC parameters, the reader should refer to the appropriate manufacturers' datasheets.

2.2 Artix Bank Pin Assignments

The following figure shows the bank pin assignments on the FPGA followed by a table that shows the detail I/O connections. The XC7A50T-FTG256 device has 4 I/O banks.

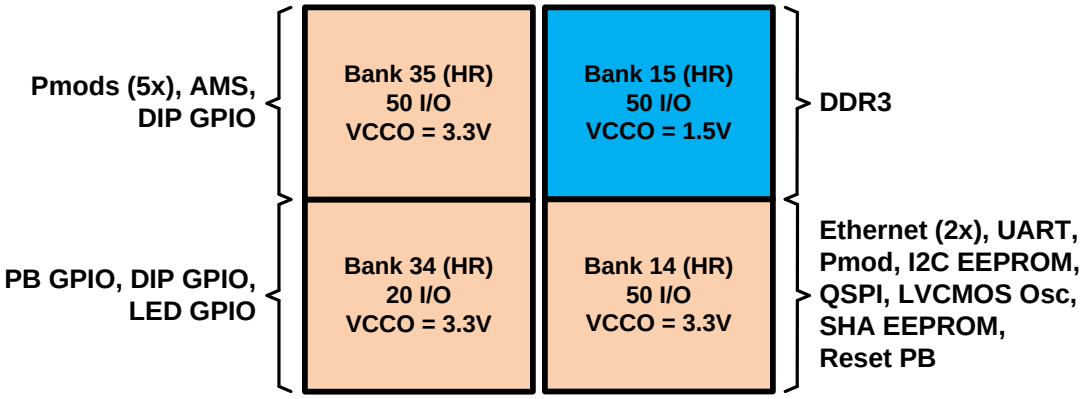

Figure 3 – Artix 7A50T Bank Assignments

The following table shows the complete bank pin assignments for the Xilinx 7A50T-FTG256 FPGA.

Bank	I/Os used	Usage
14 3.3V	13	Ethernet 1 (RMII, Link, GPIO)
	13	Ethernet 2 (RMII, Link, GPIO)
	2	UART
	8	Pmod
	2	I2C EEPROM
	6	QSPI
	1	SHA EEPROM
	1	Reset PB Switch
	1	PUDC_B pin
	1	LVCMOS 200MHz System Clock
	48	***Total bank I/O (50 max. I/O)***
15 1.5V	47	DDR3
	47	***Total bank I/O (50 max. I/O)***
34 3.3V	4	PB GPIO
	4	DIP GPIO
	10	LED GPIO
	18	***Total bank I/O (20 max. I/O)***
35 3.3V	40	Pmods
	4	DIP GPIO
	4	AMS
	48	***Total bank I/O (50 max. I/O)***

Table 1 – FPGA Bank Pin Assignments

2.3 Memory Interfaces

The Artix-7A50T board will provide memory interfaces to DDR3 SDRAM and SPI Flash.

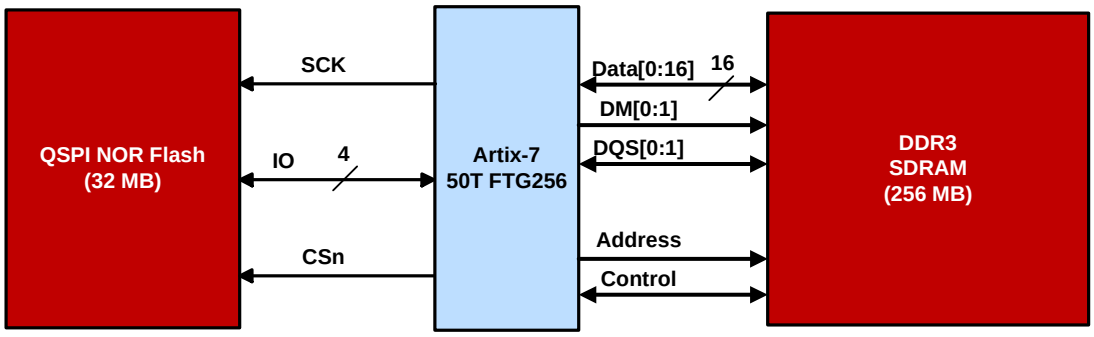

Figure 4 - Development Board Memory Interfaces

2.3.1 32MB QSPI Flash Interface

The Artix-7A50T board has 32 MB of Quad SPI FLASH to store FPGA configuration and user application software/data. The QSPI is either a Micron N25Q256A13ESF40G or Spansion S25FL256SAGMFI001 Multi-bit SPI Flash (x4 data).

The FPGA CCLK is a dedicated pin that clocks during FPGA configuration but then tri-states when FPGA configuration is complete. To enable QSPI access while the board is running in non-configuration mode, a second clock pin EMCCLK14 is provided via R32 to the QSPI SCK pin. This pin is in a tri-state mode during configuration which prevents contention on the SCK pin.

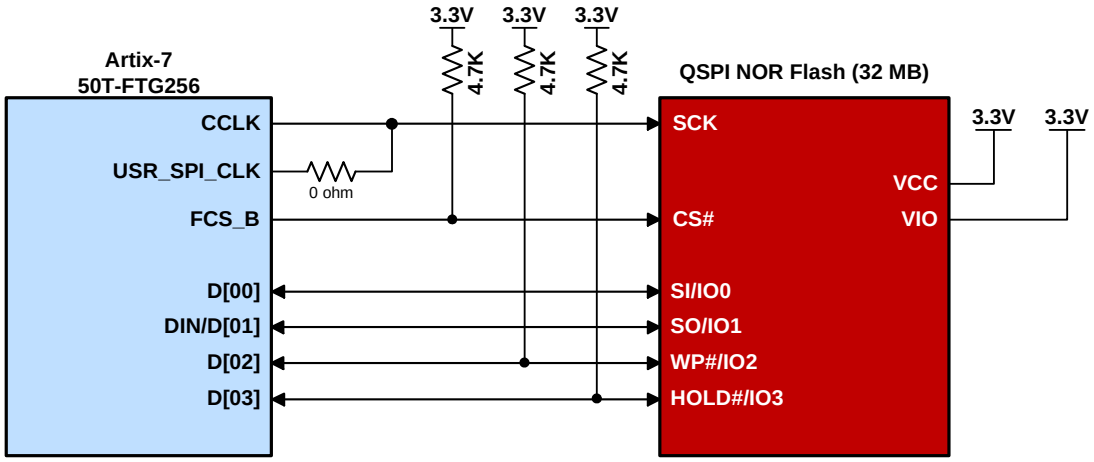

Figure 5 – Quad SPI Flash Interface

2.3.2 256MB DDR3 Memory Interface

The Artix-7A50T board has a 256 MB DDR3 SDRAM (128M x16) memory IC (Micron MT41K128M16JT-125 96-ball FBGA package (1.35V/1.5V, 128M16, 1600Mbps) installed by default. Alternatively, the design can accommodate a Micron MT41K128M16JT-107. The following figure shows the DDR3 interface on the Artix-7A50T board. JT11, a 40.2 ohm 0402 resistor at location 1-2, is used to configure the ODT (On Die Termination) for the memory interface.

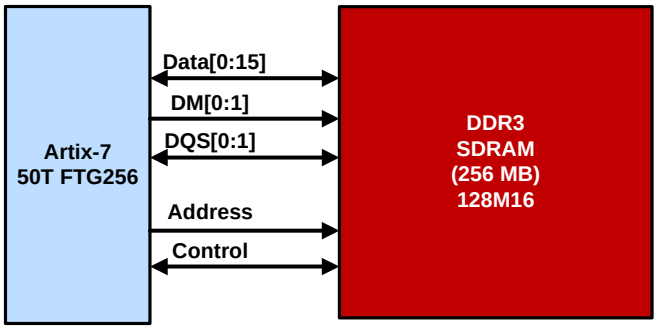

Figure 6 – DDR3 Memory Interface

The table below shows bank 15s DDR3 interface pin assignments used on the Artix-7A50T board. This pinout was created using the Xilinx Memory Interface Generator (MIG) v2.0 in the Vivado version 2013.4 tools. To save an FPGA I/O, the DDR3 device CS# pin is pulled low on the PCB to permanently enable the DDR3 memory. Additionally, the FPGA uses the internal reference voltage (Vref).

IO Bank	Pin Name	Pin Number	Signal Name
15	IO_L13P_T2_MRCC_15	E12	ddr3_dq[0]
15	IO_L13N_T2_MRCC_15	E13	ddr3_dq[1]
15	IO_L14P_T2_SRCC_15	E11	ddr3_dq[2]
15	IO_L14N_T2_SRCC_15	D11	ddr3_dq[3]
15	IO_L16N_T2_A27_15	F13	ddr3_dq[4]
15	IO_L17P_T2_A26_15	E16	ddr3_dq[5]
15	IO_L17N_T2_A25_15	D16	ddr3_dq[6]
15	IO_L18P_T2_A24_15	F15	ddr3_dq[7]
15	IO_L19N_T3_A21_VREF_15	G12	ddr3_dq[8]
15	IO_L20P_T3_A20_15	H12	ddr3_dq[9]
15	IO_L20N_T3_A19_15	H13	ddr3_dq[10]
15	IO_L22P_T3_A17_15	H16	ddr3_dq[11]
15	IO_L22N_T3_A16_15	G16	ddr3_dq[12]
15	IO_L23P_T3_FOE_B_15	J15	ddr3_dq[13]
15	IO_L23N_T3_FWE_B_15	J16	ddr3_dq[14]
15	IO_L24P_T3_RS1_15	H14	ddr3_dq[15]
15	IO_L1P_T0_AD0P_15	C8	ddr3_addr[13]

15	IO_L1N_T0_AD0N_15	C9	ddr3_addr[12]
15	IO_L2P_T0_AD8P_15	A8	ddr3_addr[11]
15	IO_L2N_T0_AD8N_15	A9	ddr3_addr [10]
15	IO_L4P_T0_15	B10	ddr3_addr [9]
15	IO_L4N_T0_15	B11	ddr3_addr [8]
15	IO_L5P_T0_AD9P_15	B12	ddr3_addr [7]
15	IO_L5N_T0_AD9N_15	A12	ddr3_addr [6]
15	IO_L6P_T0_15	D8	ddr3_addr [5]
15	IO_L6N_T0_VREF_15	D9	ddr3_addr [4]
15	IO_L7P_T1_AD2P_15	A13	ddr3_addr[3]
15	IO_L7N_T1_AD2N_15	A14	ddr3_addr[2]
15	IO_L8P_T1_AD10P_15	C14	ddr3_addr[1]
15	IO_L8N_T1_AD10N_15	B14	ddr3_addr[0]
15	IO_L9P_T1_DQS_AD3P_15	B15	ddr3_ba[2]
15	IO_L9N_T1_DQS_AD3N_15	A15	ddr3_ba[1]
15	IO_L10P_T1_AD11P_15	C16	ddr3_ba[0]
15	IO_L10N_T1_AD11N_15	B16	ddr3_ras_n
15	IO_L11P_T1_SRCC_15	C11	ddr3_cas_n
15	IO_L11N_T1_SRCC_15	C12	ddr3_we_n
15	IO_L18N_T2_A23_15	E15	ddr3_reset_n
15	IO_L12P_T1_MRCC_15	D13	ddr3_cke
15	IO_L12N_T1_MRCC_15	C13	ddr3_odt
15	IO_L16P_T2_A28_15	F12	ddr3_dm[0]
15	IO_L19P_T3_A22_15	H11	ddr3_dm[1]
14	IO_L13P_T2_MRCC_14	N11	sys_clk_i
15	IO_L15P_T2_DQS_15	D14	ddr3_dqs_p[0]
15	IO_L15N_T2_DQS_ADV_B_15	D15	ddr3_dqs_n[0]
15	IO_L21P_T3_DQS_15	G14	ddr3_dqs_p[1]
15	IO_L21N_T3_DQS_A18_15	F14	ddr3_dqs_n[1]
15	IO_L3P_T0_DQS_AD1P_15	B9	ddr3_ck_p[0]
15	IO_L3N_T0_DQS_AD1N_15	A10	ddr3_ck_n[0]

Table 2 – DDR3 Pin-out for the On-board 128Mx16 Interface

2.3.3 32KB I2C EEPROM

A ST Microelectronics M24C32 32KB I2C EEPROM is placed for storing board level parameters and system settings such as EtherCAT device data.

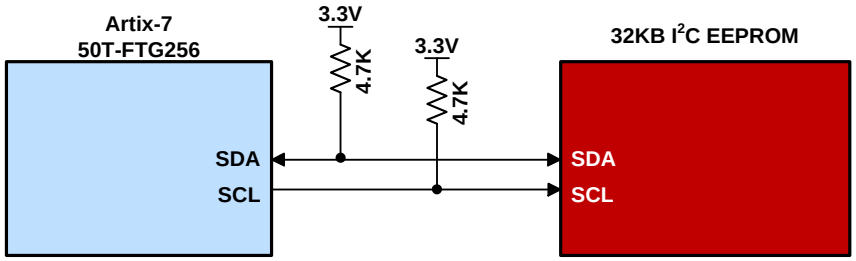

Figure 7 - I²C EEPROM Interface

2.4 Dual 10/100 Ethernet PHYs

The Artix-7A50T board has two TI 83630 PHYs providing two 10/100 Ethernet ports for network connection and for operation with Industrial Ethernet protocols. The DP83630 includes hardware IEEE1588 support. Each PHY interface is configured as a slave using RMII instead of MII to save on FPGA pin connections. A 2.2K ohm resistor is used in the below JT configurations at the specified location.

- JT10/JT16, locations 1-2, is pulled-up and used on the CRS_DV signal to configure the LED interface.
- JT9/JT15, locations 1-2, is pulled-up resistor on RX_DV/MODE signal to configure the PHY for RMII mode.
- JT6/7/8 & JT12/13/14 set the address of the of the PHYs. PHY1 address is 0x11 and PHY2 address is 0x10.
- JP1 and JP2 are used on the PHYs GPIO1 pins to enable the PHY clock output (default). This pin also doubles as a user clock input, so a jumper is provided to prevent contention.
- J3 and J5 are standard 100 mil pitch headers to provide the user with PHY GPIO access.

A high-level block diagram of the 10/100 Ethernet interface is shown in the following figure.

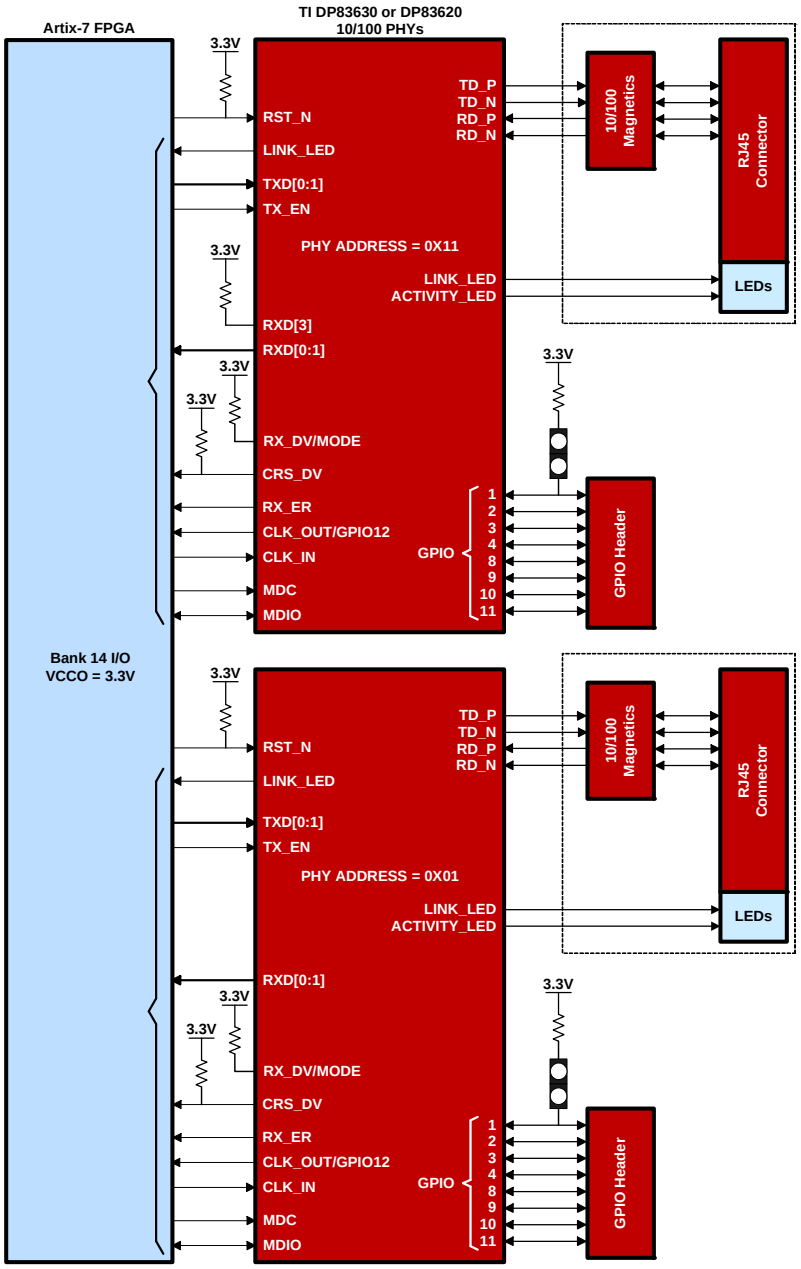

Figure 8 – 10/100 Ethernet Interfaces

2.5 XADC Support

The Artix-7A50T board supports Xilinx's XADC functionality as shown in the below figure:

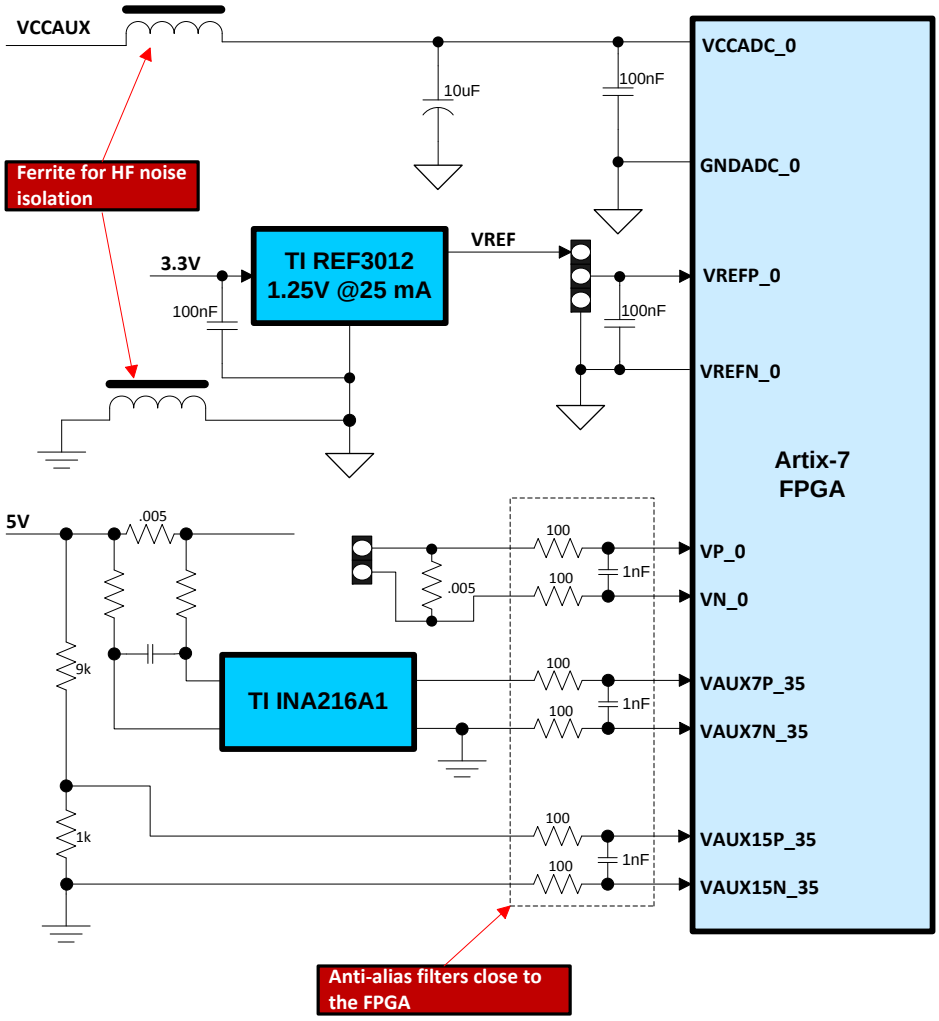

Figure 9 - XADC Support Circuitry

Note: The VREF jumper can be used to set the VREFP for external (output of the REF3012) or internal operation.

2.5.1 ADC Configuration Selections and operational notes:

- JP7 provides a means in which to select the internal A/D converter's reference voltage. A TI precision REF3012, 1.25V, 50 ppm reference IC and ground are the selectable options. The default is selection is a jumper placed on pins 1-2, which is 0 volts. For 1.25V Vref, move jumper to location 2-3.

- JP8 is used to select or bypass precision trim resistor R46. By default this jumper is placed to bypass this resistor.

- Board current measurement: U10 and R79 are used to measure the boards input current. U10 is a precision difference amplifier with low input offset voltage to ensure accurate readings on the A/D interface.

- Voltage in measurement: R88/R89 provides an approximate 10:1 voltage divider input.

2.6 USB-UART Port

The USB UART port provides two functions. One is to power the board in low power applications (less than 2.5 Watts via a PC USB connection) and the other is to interface to the FPGA via a command terminal window such as TeraTerminal. This interface can, however, support up to 1 amp input. The user would have to provide the appropriate USB power supply for this.

The USB UART used is the Silicon Labs SiLabs CP2104. Through the options provided on the Artix 7A50T board this interface can be configured in many different manners. Please refer to the Silicon Labs CP2104 datasheet for further information. The Avnet default mode is Device Mode, with an interface configuration of 115,200, 8, N, 1. LED D6 is provided to indicate a link has been made with the USB host.

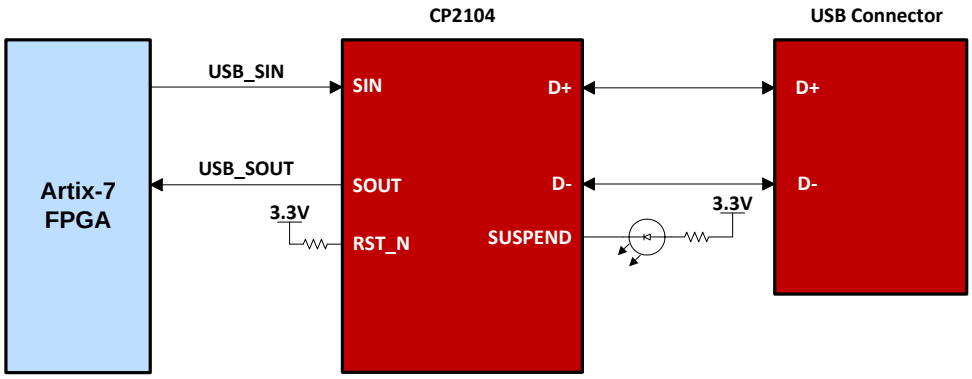

Figure 10 - USB UART Interface

2.7 DIP and PB Switches

There are multiple user and ID switches available on the Artix 7A50T board.

- SW7: 4 position slide switch (can be used for Node ID with the PowerLink IE protocol).
- PB SW 1 – 4: user push button switches, active high.
- SW6: 4 position slide switch (can be used for Node ID with the PowerLink IE protocol).
- PB SW8: MicroBlaze CPU reset, active high.
- PB SW5: PROG_PB FPGA reconfiguration, active low.

2.8 User LEDs

- 8 user LEDs, D11-D18. A logic high on the FPGA I/O causes the LED to turn on.
- 2 Ethernet status LEDs D7 and D8 (active low)are used with Industrial Ethernet protocols to indicate an error condition and link status. These LEDs are driven from the IE MAC IP in the FPGA. The remaining 8 LEDs are general purpose.
- 1 FPGA Configuration Done Blue LED (D10).
- 1 USB UART Connected Yellow LED (D6).

2.9 SHA EEPROM

The Artix-7A50T board provides a SHA-256 Security EEPROM for FPGA authentication using the Maxim DS28E15 device. This interface requires 1 FPGA I/O and one pull-up resistor. Refer to Maxim's website for further use information.

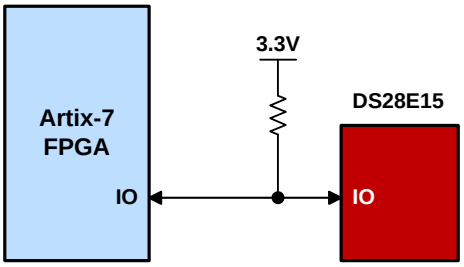

Figure 11 – SHA-1 EEPROM 1-Wire Interface

2.10 Peripheral Module (PMOD) I/O Expansion Headers

The Artix-7A50T board has six right-angle female I/O headers compatible with the Digilent Peripheral Module (PMOD) standard. This standard specifies 8 user I/Os plus 3.3V and ground as show in the figure below.

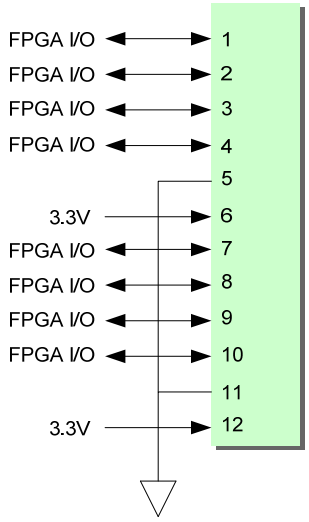

Figure 12 - PMOD Connector Pinout

A few links to PMOD product examples are provided:

- http://www.digilentinc.com/Products/Catalog.cfm?NavPath=2,401&Cat=9
- http://www.digilentinc.com/Pmods/Digilent-Pmod_%20Interface_Specification.pdf
- http://www.avnet.com/ search for TI Com8 WiFi modules

2.10.1 6 PMOD Interface Headers

Six PMOD connectors are placed in bank 35 as shown. To allow for maximum peripheral connection flexibility, the connectors are spaced appropriately and separated into pairs. There are two PMOD connectors per pair and three sets total. To ensure maximum data path performance all PMOD connector pins have are connected to the FPGA differentially (<P|N> pairs) and routed at 100 ohm differential impedance.

- Pair J7 & J8: bank 35, differential signaling with anti-alias filtering to allow for high sensitivity peripherals to be placed
- Pair J6 & J11: bank 35, standard differential signaling
- Pair J9 & J10:
  - J9: bank 35, standard differential signaling
  - J10: differential signaling with anti-alias filtering to allow for high sensitivity peripherals to be placed.

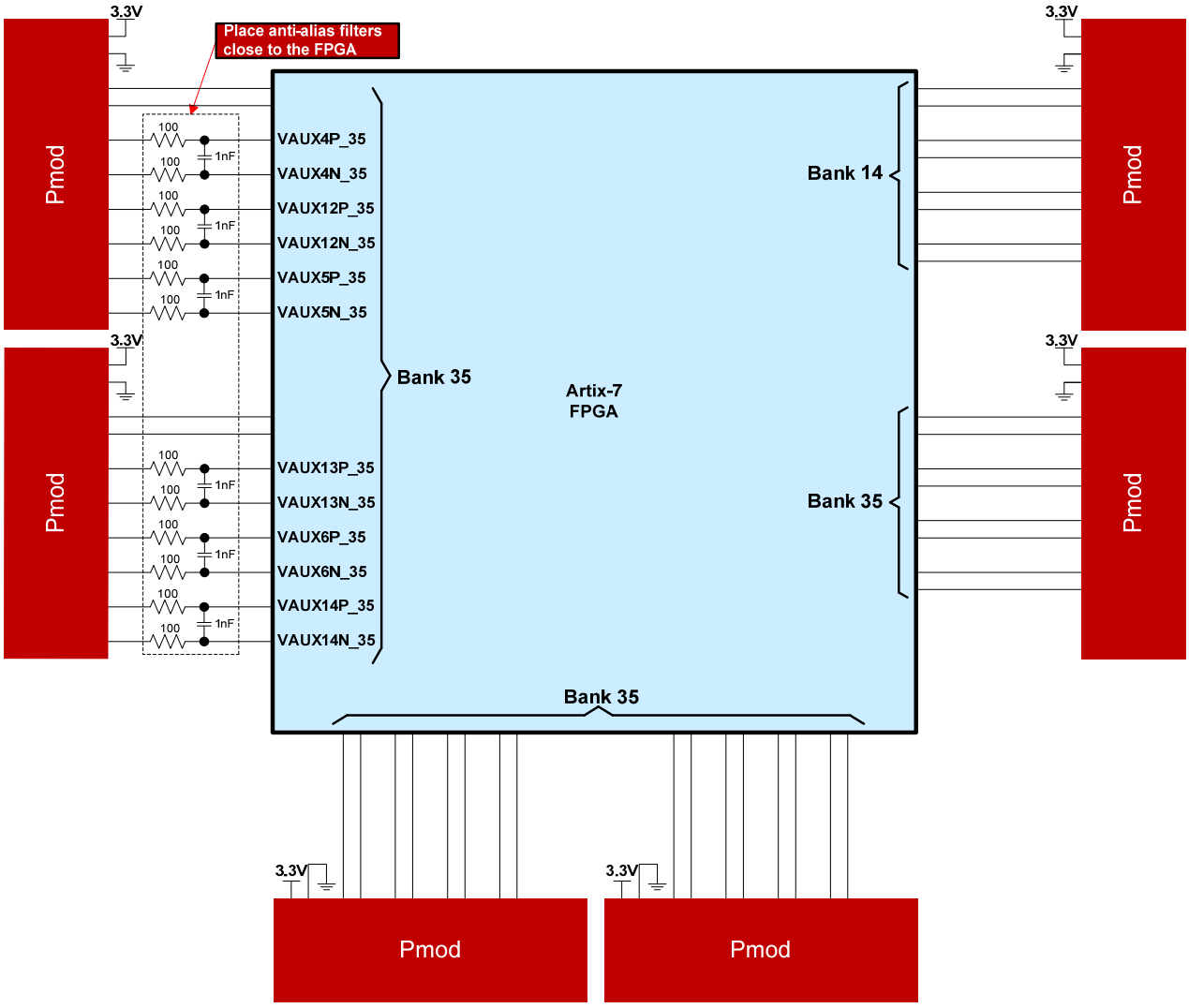

Figure 13 - PMOD Placement

2.11 Boot Configuration Mode

The Artix-7A50T board uses a Micron (N25Q256A13ESF40G) or Spansion (S25FL256SAGMFI001) Multi-bit (x4 data) QSPI Flash device for FPGA configuration. The QSPI Flash device is connected to the FPGA in Master SPI mode as shown in the following figure.

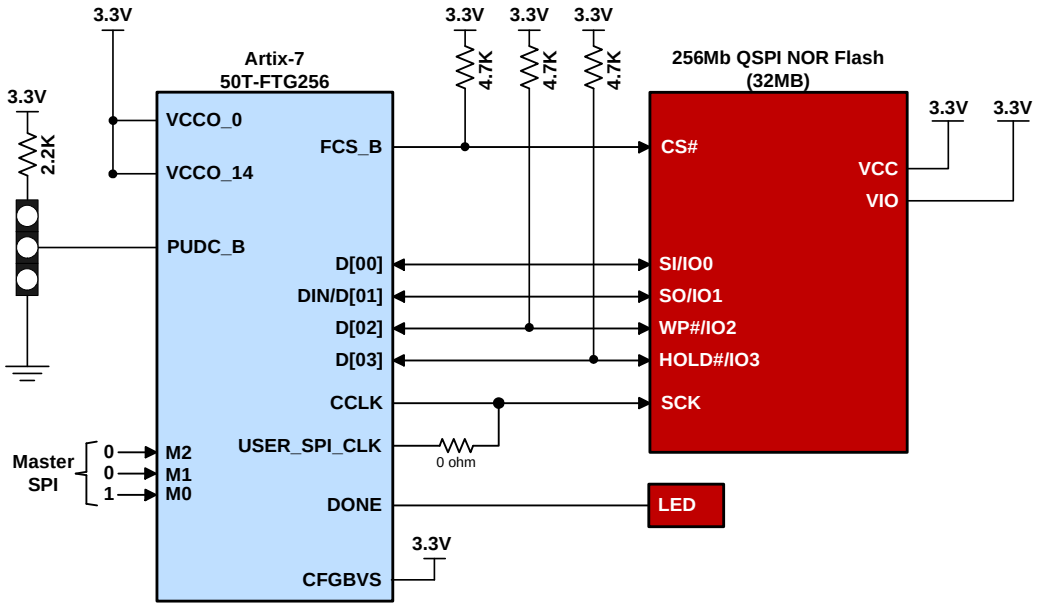

Figure 14 - FPGA Master SPI Configuration Interface

- Boot Mode Configuration: JT18-20: the Artix-7 FPGA configuration mode pins (M[2:0]) are strapped via JT18-20 pull-up and pull-down resistors to set the configuration mode to Master SPI (M[2:0] = “001”).

- JP6: PUDC: the Pull Up During Configuration active-low (PUDC_B) pin is pulled up to V_{CCO_14} via 2.2K ohm resistor with the option to tie it to ground via a post header.

2.12 JTAG Chain

The Artix 7A50T board has the Digilent SMT2 JTAG module and Xilinx PC4-style JTAG port connector (not populated) for configuration of the FPGA and indirect programming of the on-board SPI configuration Flash. The following figure shows the JTAG chain on this development board.

Artix-7 devices have a dedicated four-wire JTAG port that is always available to the FPGA regardless of the mode pin settings.

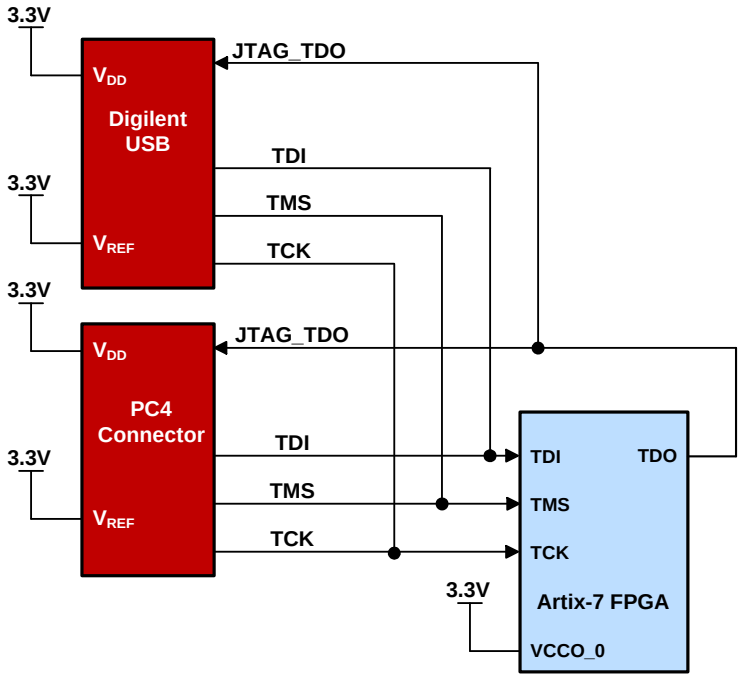

Figure 15 - JTAG Chain

2.13 Clock Connections to the Artix-7 FPGA

The following figure shows clock connections to the Artix-7 FPGA.

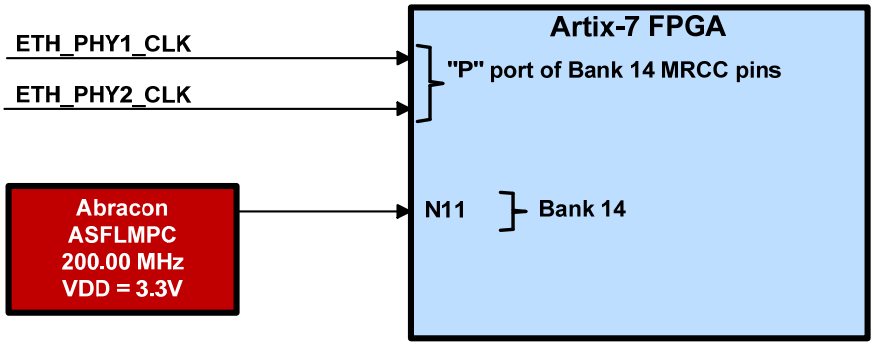

Figure 16 - Clock Connections to the FPGA

2.14 Power Connections to the Artix-7 FPGA

The following figure shows the power connections to the Artix-7 FPGA.

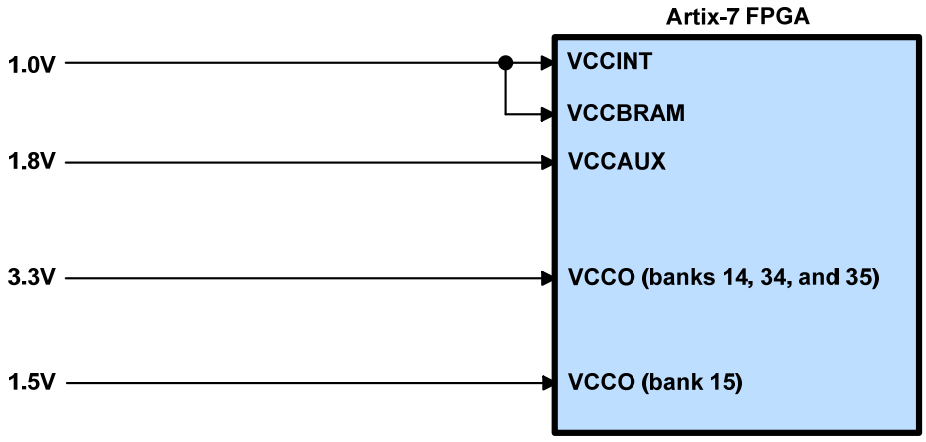

Figure 17 - FPGA Power Connections

2.15 FPGA V_{CCBAT} Connection

In the event a user wants to use encryption, the board features a 11.5mm LR44 coin cell battery holder. This battery is used to maintain Vccbat power when the primary input power is removed. This battery is not required to be placed for normal board operation. A non-rechargeable (primary) battery is recommended to be placed as the board does not contain a recharging circuit for secondary batteries. Additionally, a blocking diode is placed to prevent the 1.8V power supply from putting a charge onto this battery. The absolute maximum input voltage is 2.00 volts.

2.16 Power Requirements

The following table shows the power requirements on the Artix-7A50T board. The input voltage is 5.0V, +/- 10% via the Micro USB connector or the Barrel connector.

Device	Voltage (+/- 5%)	Current	Comment
Artix-7 Core	1.0V		
IO	3.3V		FPGA I/O
VCCAUX	1.8V		
PMOD Connectors	3.3V	0.8A	FPGA I/O ((20mA/pin * 8 pins/Pmod) * 6 Pmods)
DDR3	1.5V		
Vccbatt	<1.89V	10mA	Optional encryption backup power.

Table 3 - Power Supply Requirements

2.16.1 Internal board power:

The 7A50T board features an Analog Devices AD5052 five regulator IC. This IC provides all of the board's internal power as depicted:

- CH1: 1.0V @ 2.0A
- CH2: 3.3V @ 2.0 A
- CH3: 1.2V @ 1.0 A
- CH4: 1.8V @ 1.0 A
- CH5: 1.8VADC LDO out. Filtered 1.8V supply for XADC

2.16.2 Power Connections

There are two methods in which to power the Artix 7A50T board.

- Micro USB type B input connector, J1
  Primary +5V USB power input supplied by a PC or a USB wall adapter power supply with a current rating of 1 amp or greater.

- Barrel Jack, J13 + D21
  - 5.5mm x 2.5mm center positive barrel jack for high current I/O applications. Secondary/supplemental power input. Diode D21 is used as a steering diode to prevent back-feed with the micro USB connection.

2.16.3 Analog Devices Switch Mode power supply, U13:

- ADI5052 four channel SMPS+1 channel LDO (five total regulators)
  - Configured for forced PWM switching via R91.
  - Configured for a soft-start delay of 2mS via R119 and R120.
  - Resistor adjustable DDR bank voltage for 1.3V or 1.5V VDDR (1.5V default). See schematic for configuration options.

2.16.4 Bypassing/Decoupling

The Artix 7A50T follows the recommended decoupling techniques per each manufacturer's datasheet.

3 I/O Count

The following table shows the I/O count for the Artix-7A50T board design.

Device	I/O Pins
10/100 RMII PHY (x2)	26
USB-UART	2
Push button switch GPIO	4
DIP switch GPIO (user)	4
DIP switch GPIO (device address)	4
LEDs GPIO	10
PMOD I/O Connectors	48
I2C EEPROM	2
DDR3 SDRAM	47
QSPI	6
Clock	1
SHA-256 EEPROM	1
Reset PB	1
PUDC_B	1
AMS	4
Total I/O Count	161 (Total available I/O = 170)

Table 4- Board I/O Count

4 Mechanical

4.2 Dimensions:

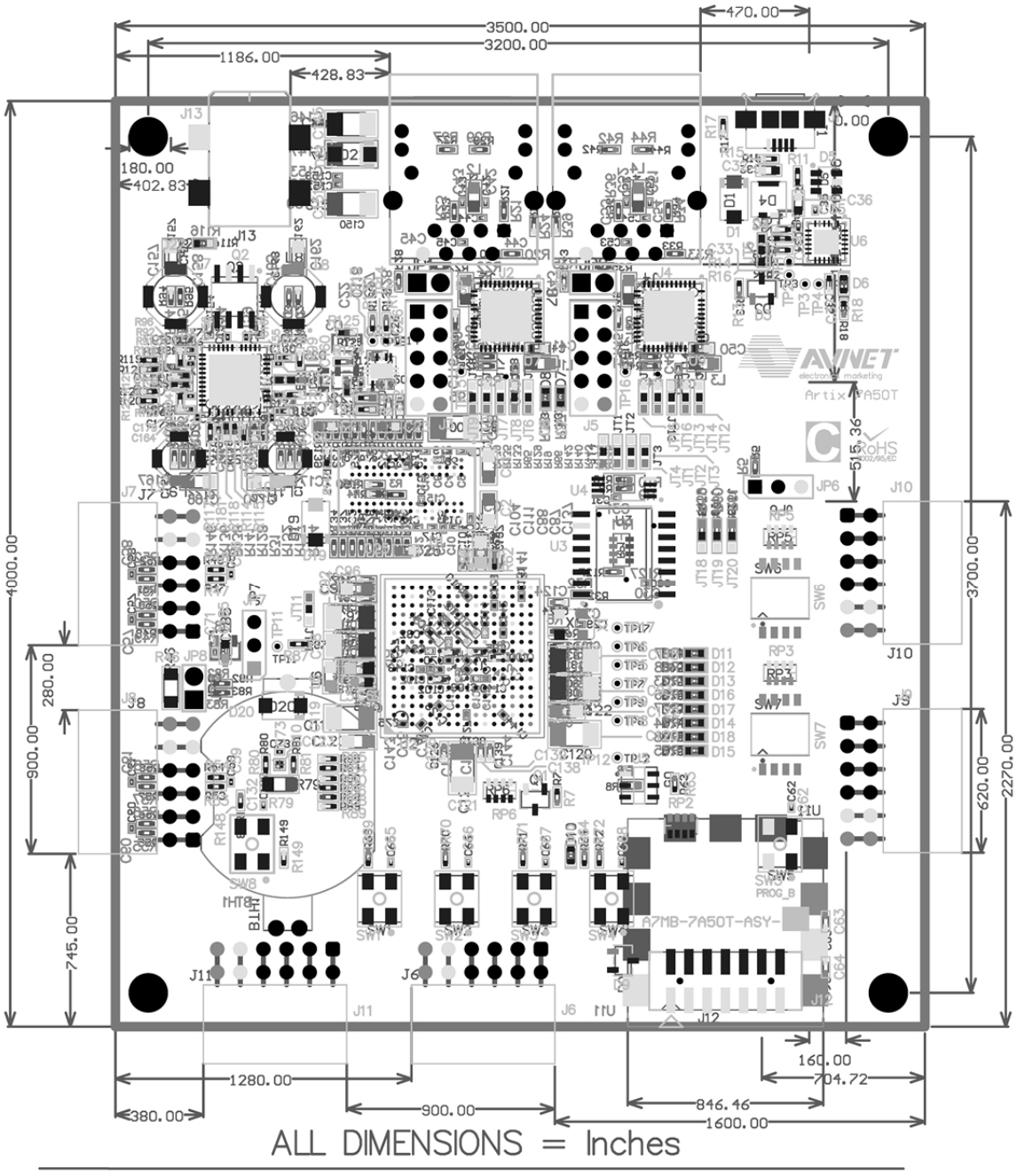

Figure 18: Top Mechanical Dimensions (mils)

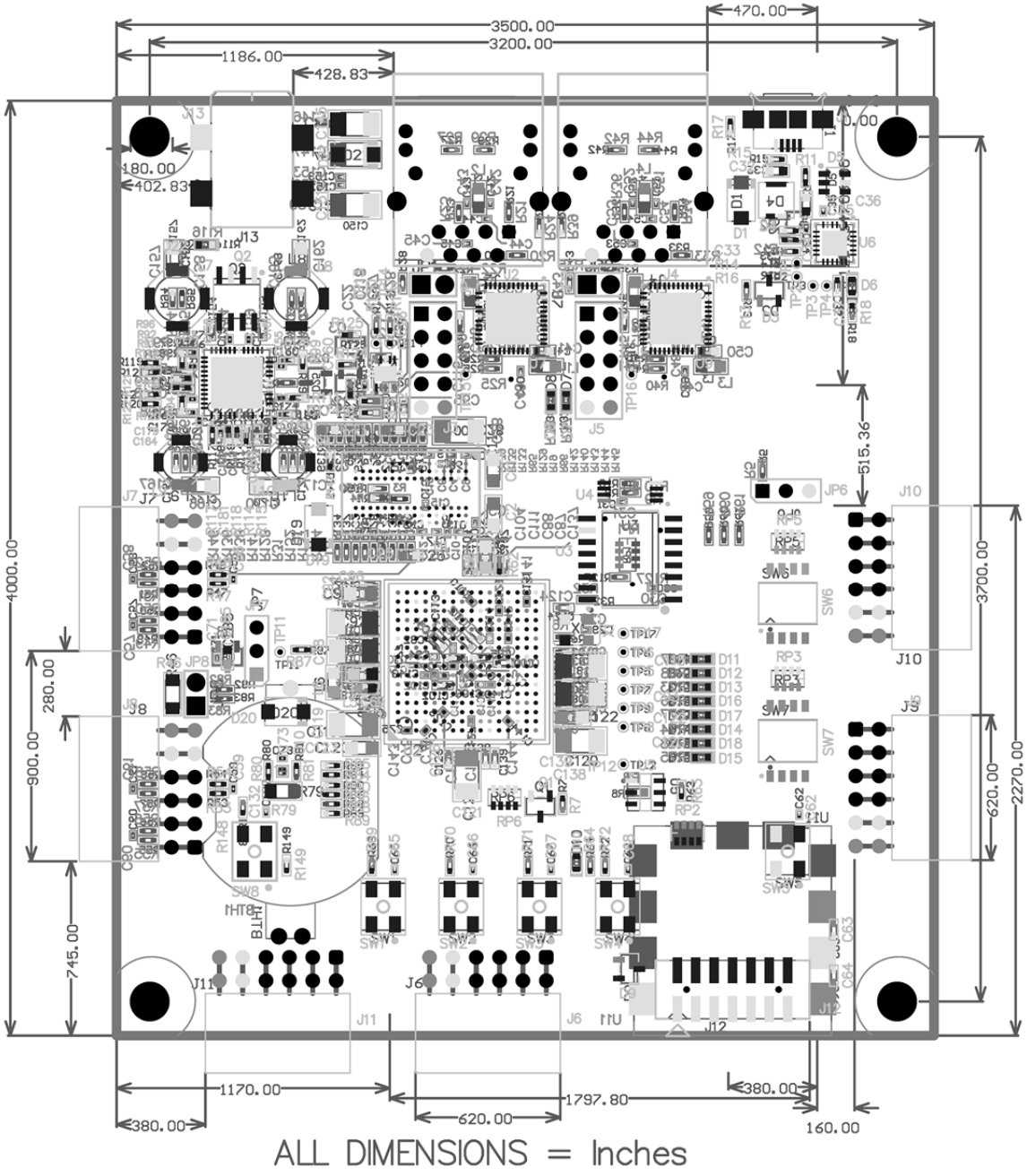

Figure 19: Bottom Mechanical Dimensions (mils)

4.2.1 Mounting Holes

There are four 125 mil diameter, plated, non-grounded mounting holes in the Artix 7A50T board.

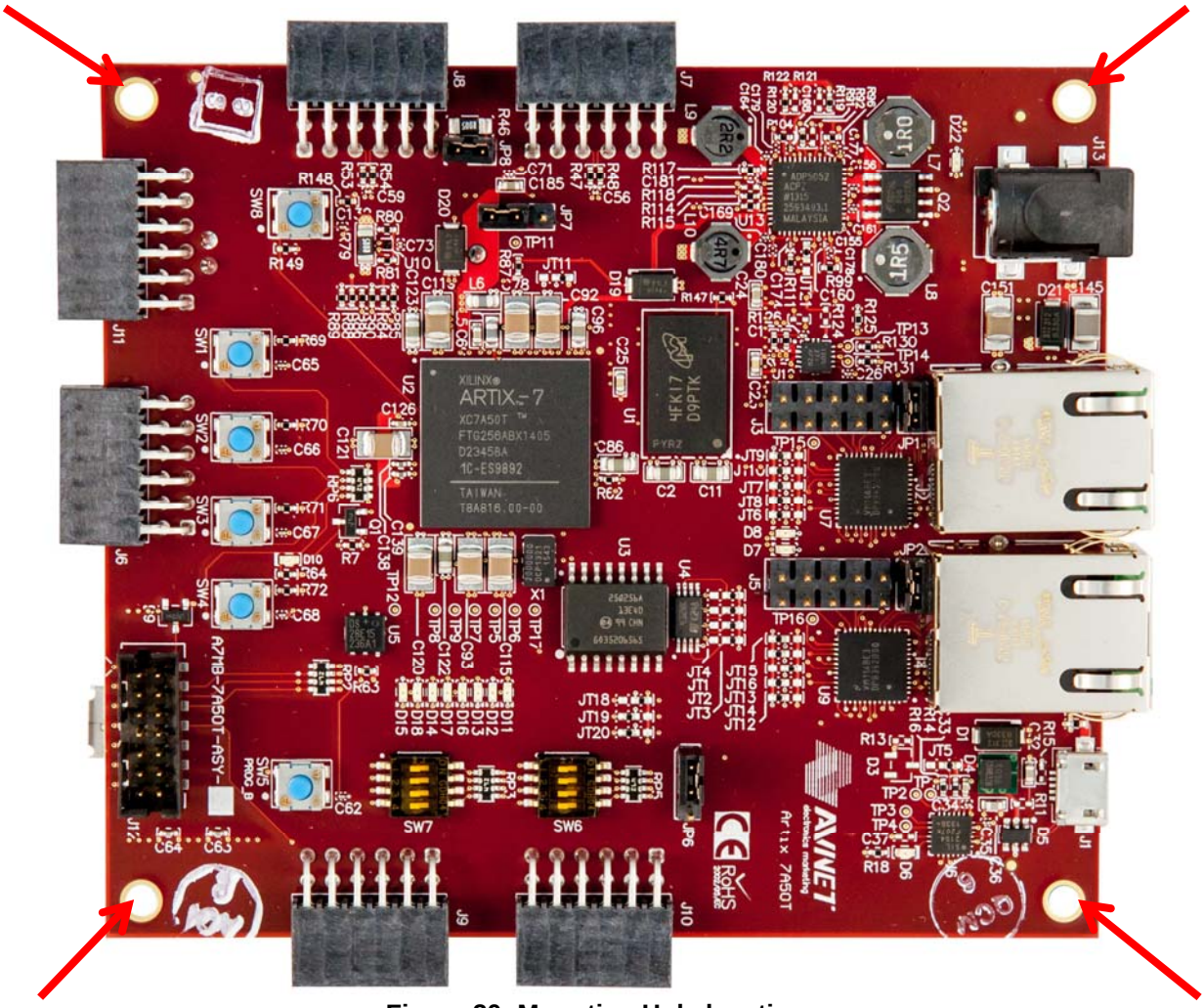

Figure 20: Mounting Hole locations

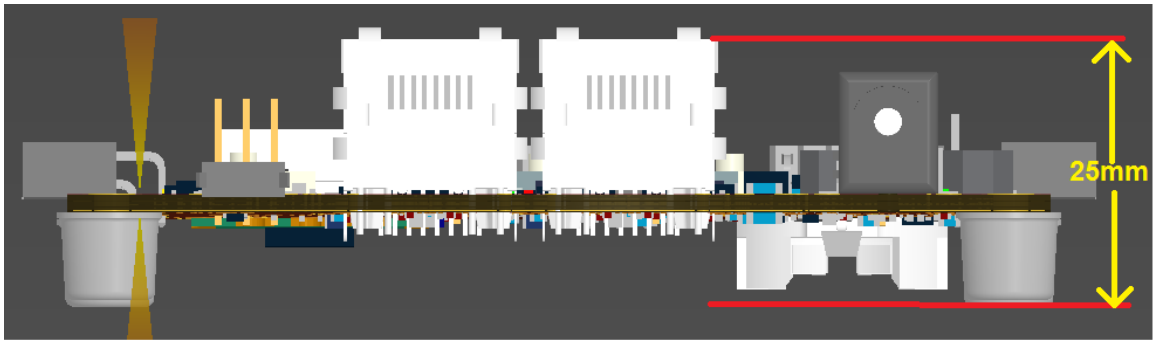

Figure 21: Artix 7A50T Vertical Mechanical Dimensions

4.3 Weight:

The weight of the Artix 7A50T with rubber feet and all jumpers populated is 5.62 OZ, 159.324 grams.

5 Revision History

Date	Revision #	Comments
03-Sep-2014	0.1	Initial draft for review.
08-Sep-2014	0.2	Review comments implemented.
23-Sep-2014	0.3	Minor formatting edits