

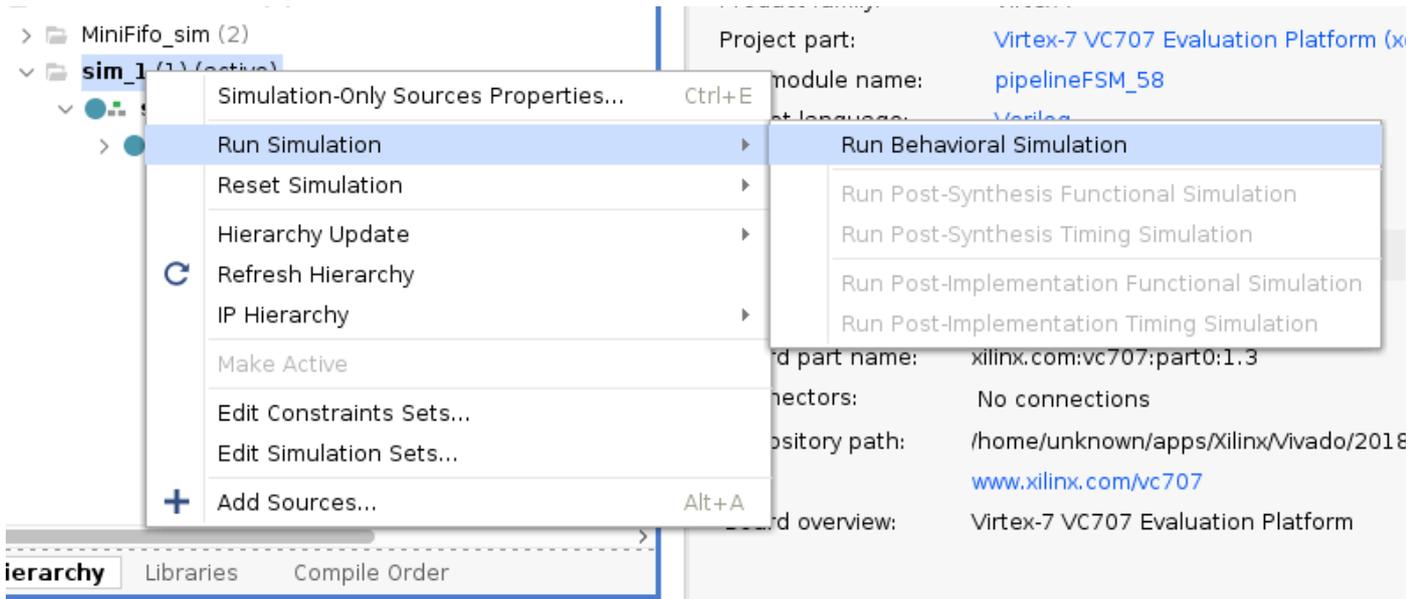
# Симуляция в XILINX Vivado

The screenshot shows the 'Sources' window in Xilinx Vivado. The 'Sources' window is divided into 'Design Sources (1)' and 'Simulation Sources (3)'. In the 'Design Sources' section, the file 'pipelineFSM\_58(pipelineFSM\_58\_synth) (pipelineFSM\_58)' is circled in red. In the 'Simulation Sources' section, the file 'sim\_1(sim\_1.sim) (1)' is circled in red, and its sub-entry 'pipelineFSM\_58\_0: pipelineFSM\_58(pipelineFSM\_58)' is also circled in red. Red arrows point from these circles to text boxes: one points from the 'pipelineFSM\_58' circle to a box containing 'Ваш модуль на VHDL или Verilog', and another points from the 'sim\_1' circle to a box containing 'Модуль теста'. The 'Flow Navigator' is visible on the left, and the 'Properties' window is at the bottom. The right side of the image shows the 'Project Settings' panel with sections for 'Settings', 'Board Parameters', and 'Synthesis'.

Ваш модуль на VHDL или Verilog

Модуль теста

# Как запустить тест на симуляцию.



# Так выглядит результат симуляции

