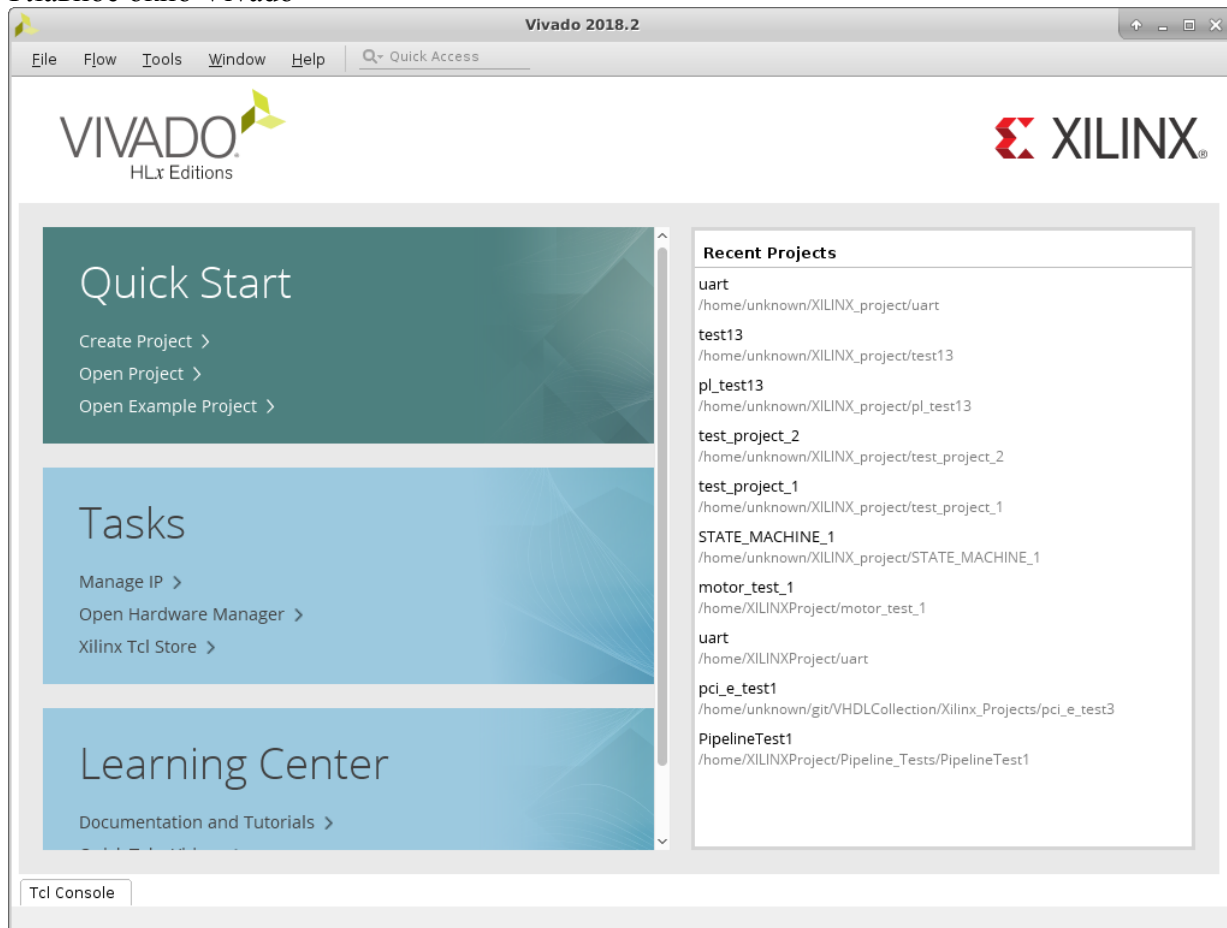
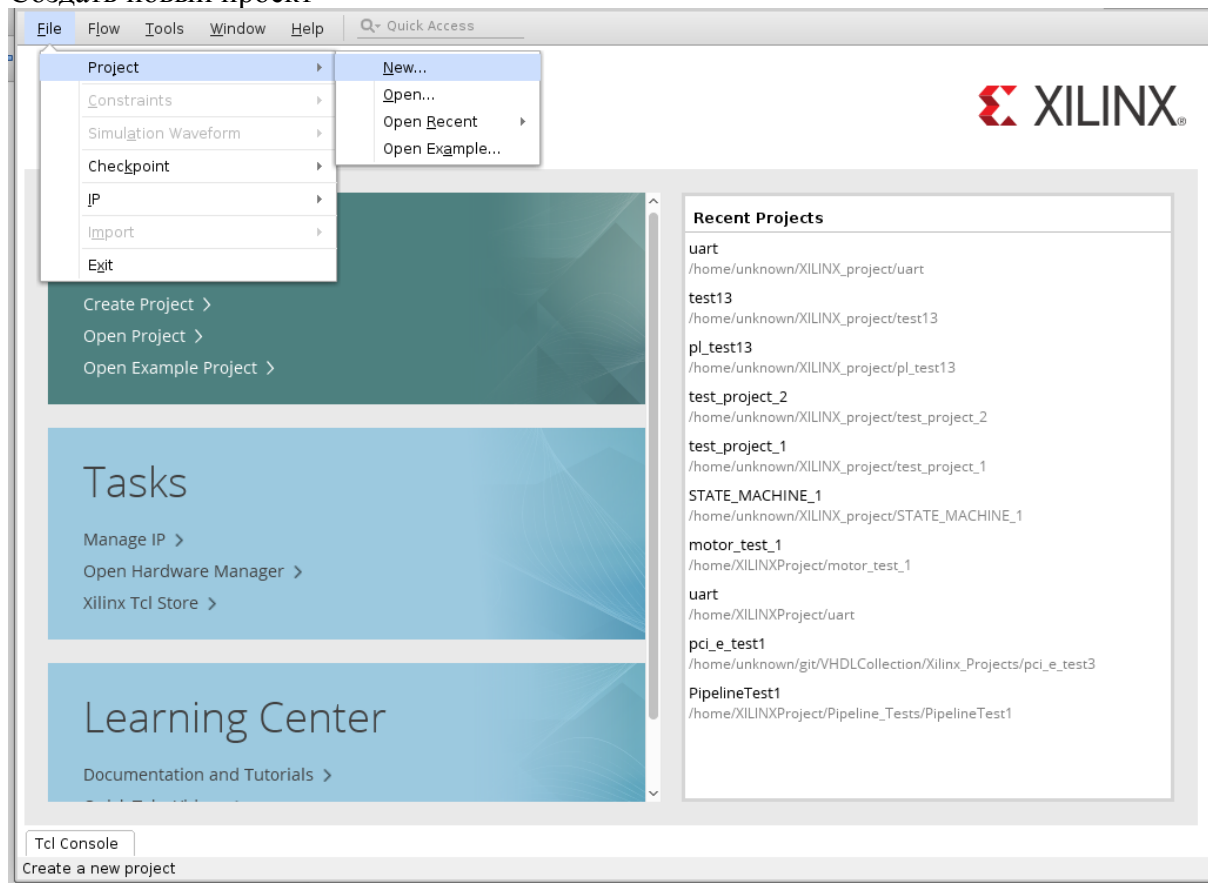


Главное окно Vivado



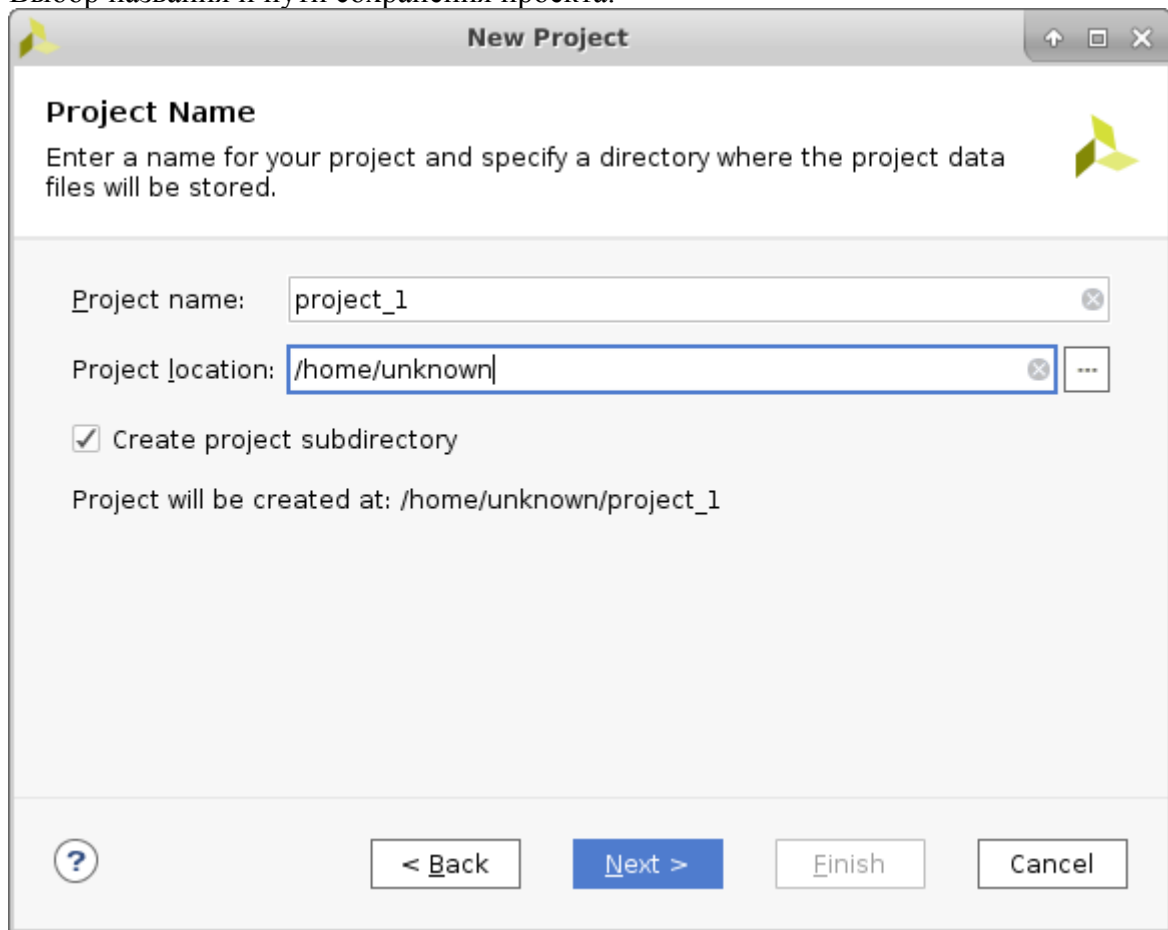
Создать новый проект



Мастер создания проекта



Выбор названия и пути сохранения проекта.



The image shows a 'New Project' dialog box with a title bar containing a yellow logo and window controls. The main area has a heading 'Project Name' and a descriptive text. Below this are two input fields: 'Project name' with the value 'project_1' and 'Project location' with the value '/home/unknown/'. The 'Project location' field has a blue border and a dropdown arrow. A checkbox labeled 'Create project subdirectory' is checked. Below the checkbox, it says 'Project will be created at: /home/unknown/project_1'. At the bottom, there is a help icon, a '< Back' button, a blue 'Next >' button, an 'Finish' button, and a 'Cancel' button.

New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

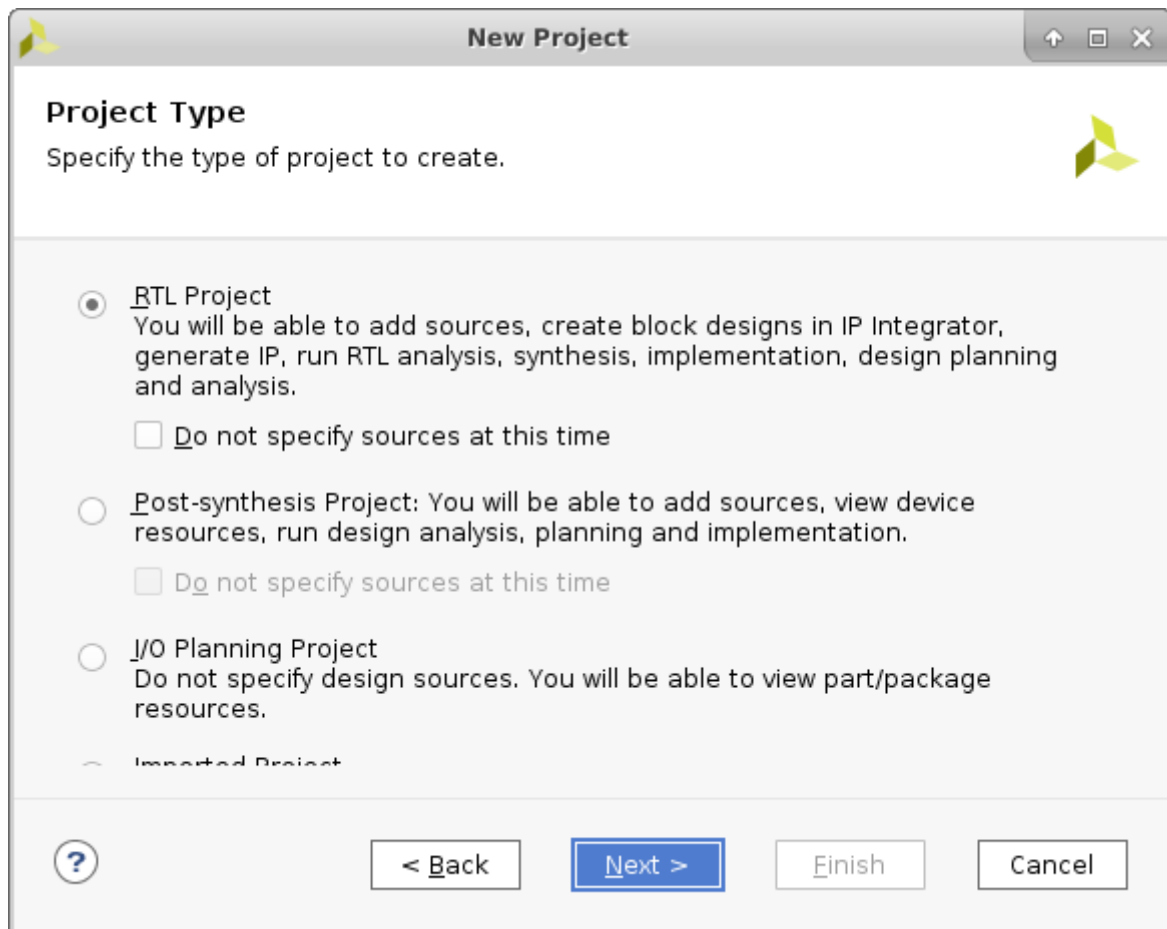
Project location:

☒ Create project subdirectory

Project will be created at: /home/unknown/project_1



Выбор типа проекта. Мы всегда будем создавать RTL проекты — это значение по умолчанию.



New Project

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time

☐ **Post-synthesis Project:** You will be able to add sources, view device resources, run design analysis, planning and implementation.

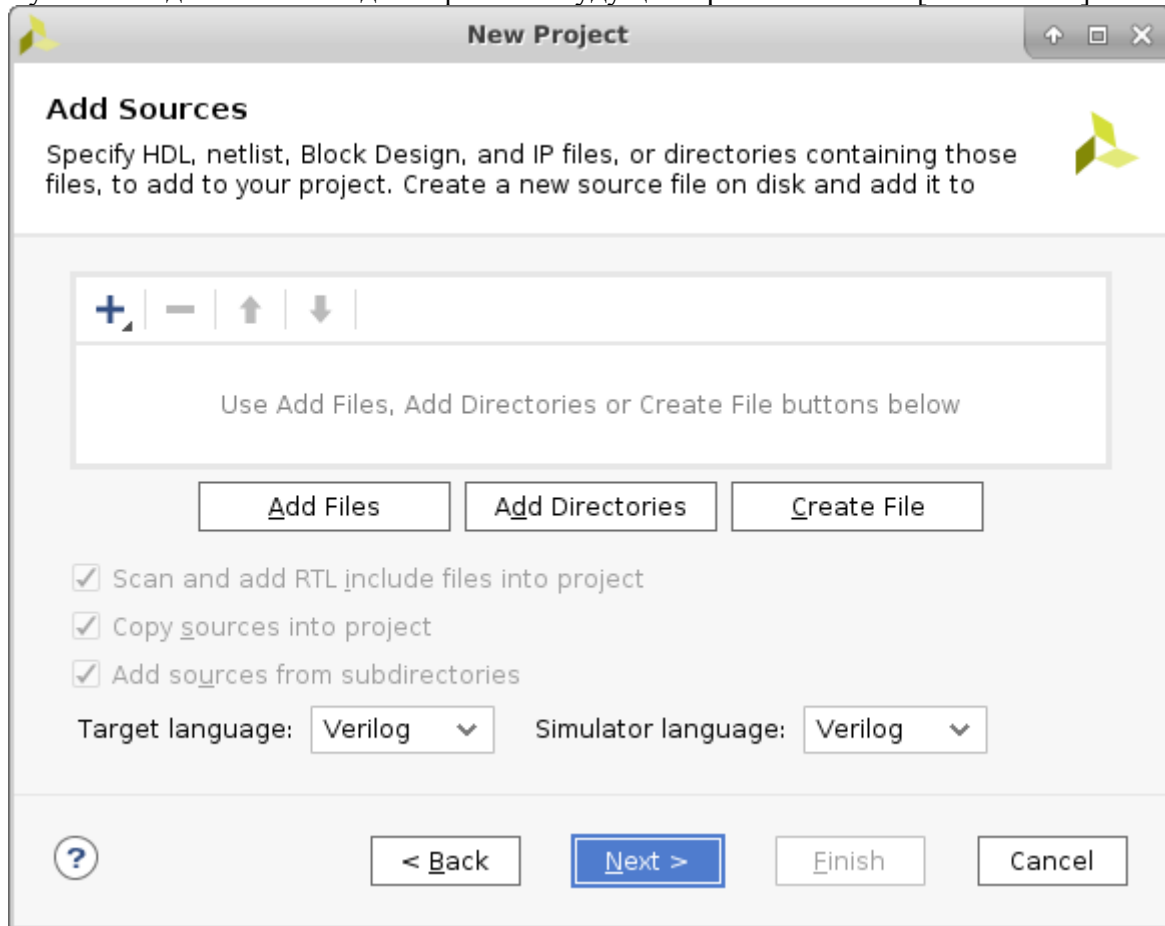
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ Imported Project

? < Back Next > Finish Cancel

Тут можно добавить исходные файлы в будущий проект. Нажать [Create File].



New Project

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to

Use Add Files, Add Directories or Create File buttons below

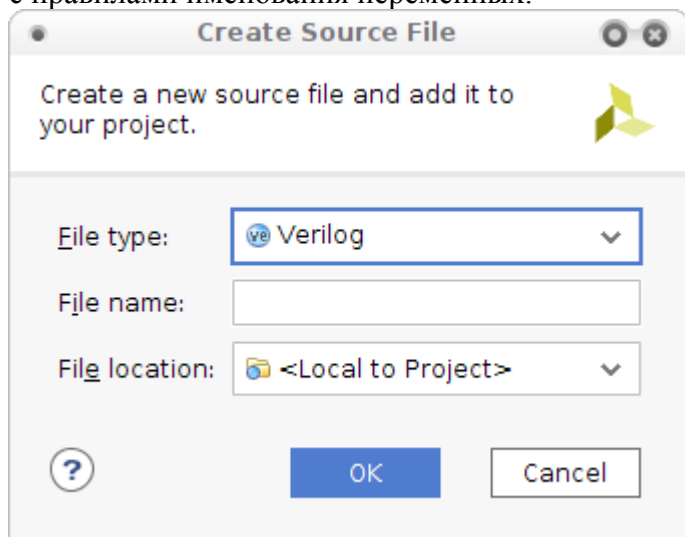
Add Files Add Directories Create File

☒ Scan and add RTL include files into project
☒ Copy sources into project
☒ Add sources from subdirectories

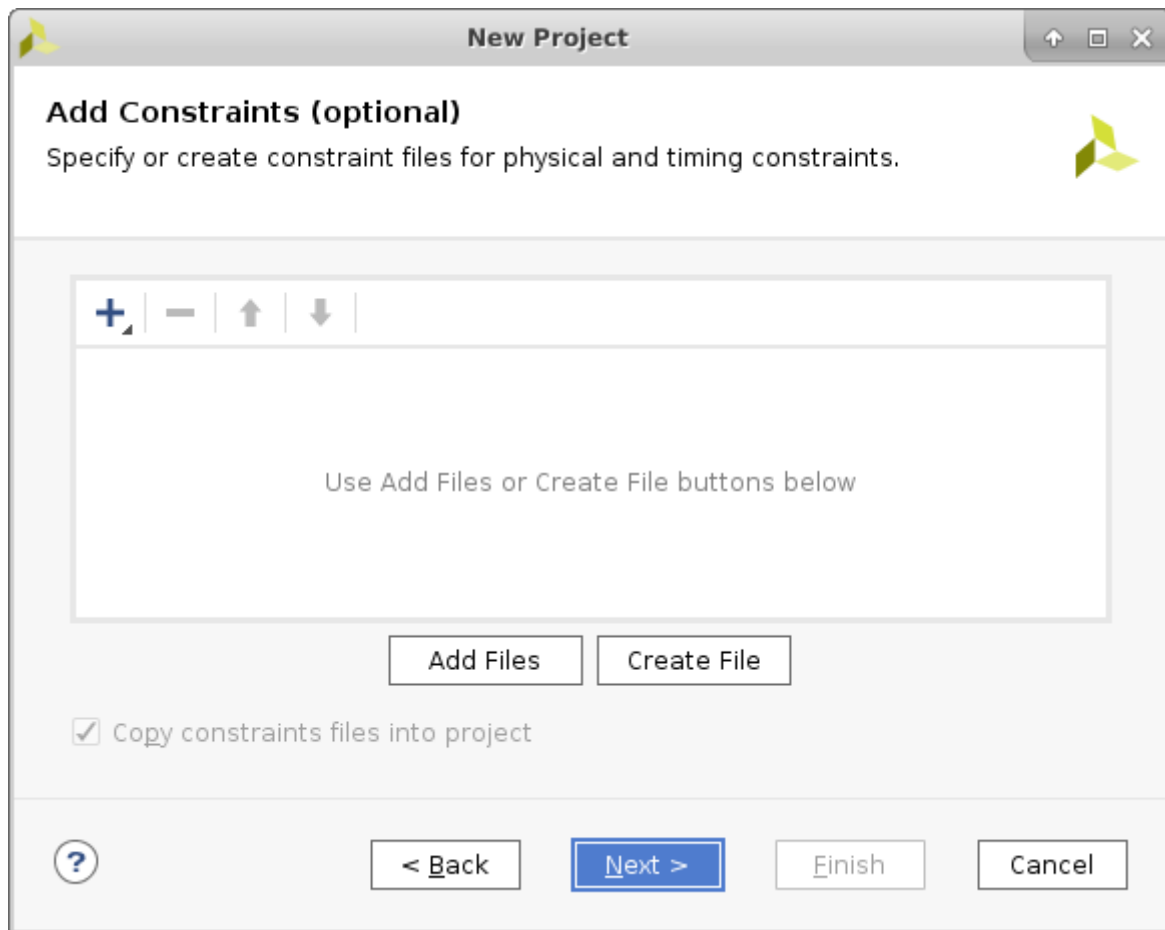
Target language: Verilog Simulator language: Verilog

? < Back Next > Finish Cancel

Тут выбираем язык, на котором будете писать, а, так же даём файлу имя в соответствии с правилами именования переменных.



Тут можно добавить в проект файлы ограничений. Именно в них будет храниться распиновка. Нажать [**Create File**].



New Project

Add Constraints (optional)

Specify or create constraint files for physical and timing constraints.

+ | - | ↑ | ↓ |

Use Add Files or Create File buttons below

Add Files Create File

☒ Copy constraints files into project

? < Back Next > Finish Cancel

Тут можно выбрать с какой именно ПЛИС мы работаем. А работаем мы именно с той ПЛИС, которая выбрана на картинке:

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

[Reset All Filters](#)

Category: General Purpose

Package: ftg256

Temperature: 1

Family: All Remaining

Speed: All Remaining

Search:

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs
xc7a15tftg256-1L	256	170	10400	20800	25	0
xc7a35tftg256-1L	256	170	20800	41600	50	0
xc7a50tftg256-1L	256	170	32600	65200	75	0
xc7a75tftg256-1L	256	170	47200	94400	105	0
xc7a100tftg256-1L	256	170	63400	126800	135	0

?

< Back

Next >

Finish

Cancel

